REMARKS

Claims 5-6 and 9-16 are pending in the application. Claims 9-16 stand rejected. Applicant gratefully acknowledges Examiner's indication that claims 5 and 6 are allowed. By the above amendment, claims 9 and 13 have been amended and claims 11, 12, 15 and 16 have been canceled without prejudice. Applicant respectfully requests reconsideration based on the above amendments and following remarks.

Specification Objections

Applicants have amended the Title to be more descriptive of the claimed inventions. Accordingly, withdrawal of the objection is requested.

Claim Rejections - 35 U.S.C. § 103

Claims 9-16 stand rejected as being unpatentable over Applicant's admitted prior art (AAPA) in view of U.S. Patent No. 5,912,463 to Mizuno et al. It is respectfully submitted that claims 9 and 12 are patentable and non-obvious over the combination of AAPA and Mizuno. Indeed, at the very least, such combination does not disclose or suggest a method that includes *compensating for loss of pixel voltage of the CMOS active pixel sensor caused by leakage current of a first photodiode connected to a gate of a first sense transistor using leakage current of a second photodiode connected to a gate of a second sense transistor complementary to the first sense transistor*, much less where the compensation is performed by *increasing the amount of current flowing to a bit line through the second sense transistor in an amount substantially proportional to the amount of decreased current flow to the bit line through the first sense transistor due to a decreased voltage of the first photodiode*, as essentially recited in claims 9 and 12.

The above features are clearly not disclosed in AAPA. Moreover, although Mizuno arguably discloses in FIG. 3 a first (110) and second (120) diode, Mizuno does not disclose or

suggest that such photodiodes are connected to gates of first and second complementary sense transistors, as essentially claimed in claims 9 and 12. Moreover, Mizuno does not disclose or suggest that compensation is performed by increasing the amount of current flowing to a bit line through the second sense transistor in an amount substantially proportional to the amount of decreased current flow to the bit line through the first sense transistor due to a decreased voltage of the first photodiode, as essentially claimed in claims 9 and 12.

In stark contrast, Mizuno discloses that the photodiodes are connected to a current signal selection circuit (150), integrating circuit (300) and differential arithmetic circuits (500). Moreover, it is clear that Mizuno discloses a fundamentally distinct process for leakage current compensation, as compared to the claimed inventions. In fact, one of ordinary skill in the art would readily recognize that due to the complexity and required layout area of the dark current compensation circuitry disclosed by Mizuno, it would be technically impractical and undesirable to implement Mizuno's circuit for each cell of a CMOS APS array.

Accordingly, for at least the above reasons, the combination of AAPA and Mizuno is legally deficient to establish a *prima facie* case of obviousness against claims 9 and 12. Moreover, claims 10 and 13 are patentable and nonobvious over such combination at least by virtue of their dependence from respective base claims 9 and 12. Therefore, withdrawal of the obviousness rejections is requested.

Respectfully submitted,

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